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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,931	TWEET ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13 and 16-19* is/are rejected.

7)☒ Claim(s) *2,14,15,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Application filed on 3/23/2004.

Currently, claims 1-21 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. Claims 3, 9, 14-16 and 18 are objected to because of the following informalities: Claims 3, 9, 16 and 18 refer to two distinct ranges (10% to 100% and 20% to 30%) and as written would not preclude percentages outside of the range to be used, the examiner suggest the claims be rewritten if the limitation of the second range is to be considered; and claims 14 and 15 recite the same limitations and are dependent from the same claim, the examiner believes the applicant wishes for one of the two claims in question to depend from claim 7. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 3-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,878,610 filed 8/27/2002) in view Fitzgerald et al. (U.S. Patent No. 6,583,015 filed 8/6/2001) and Chidambarrao et al. (U.S. Patent No. 6,881,635 filed 3/23/2004.

Lin shows the method substantially as claimed in Figs. 1-10 and corresponding text as: preparing a silicon substrate (1), including doping a bulk silicon (100) substrate (col. 2, line 56-col. 3, line 5); forming a first SiGe layer (2) on the silicon substrate (col. 2, line 56-col. 3, line 5); forming a first silicon cap on the first SiGe layer (col. 3, lines 6-11); forming a second relaxed SiGe layer on the first silicon cap (col. 3, lines 11-47); forming a second tensile-strained silicon cap on the second relaxed SiGe layer (col. 3, lines 48-58); and completing an IC device (col. 4, line 52-col. 5, line 8) (Fig. 10) (claim 1). Lin teaches that the forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300nm (col.3, lines 12-47) (claim 5). Lin teaches that the forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of

between about 10 nm to 50 nm (col. 3, lines 48-58) (claim 6). Lin shows the method substantially as claimed in Figs. 1-10 and corresponding text as: preparing a silicon substrate (1), including doping a bulk silicon (100) substrate (col. 2, line 56-col. 3, line 5); forming a first SiGe layer (2) on the silicon substrate (col. 2, line 56-col. 3, line 5); forming a first silicon cap on the first SiGe layer (col. 3, lines 6-11); and completing a CMOS device on the silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a silicon cap (col. 4, line 52-col. 5, line 8) (Fig. 10) (claim 7). Lin shows the method substantially as claimed in Figs. 1-10 and corresponding text as: preparing a silicon substrate (1), including doping a bulk silicon (100) substrate (col. 2, line 56-col. 3, line 5); forming a first SiGe layer (2) on the silicon substrate (col. 2, line 56-col. 3, line 5); forming a first silicon cap on the first SiGe layer (col. 3, lines 6-11); and completing a CMOS device on the silicon cap, wherein the CMOS device includes a source region and a drain region which are both in electrical contact with a silicon cap (col. 4, line 52-col. 5, line 8) (Fig. 10) (claim 16). Lin teaches that a second relaxed SiGe forms on the first silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer (col. 3, lines 12-58) (claim 17). Lin teaches that the forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300nm (col.3, lines 12-47) (claim 18). Lin teaches that the forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm (col. 3, lines 48-58) (claim 19).

Lin shows the method substantially as claimed and as described in the preceding paragraph.

Additionally, Lin that: the forming a first silicon cap includes forming a tensile-strained silicon cap to thickness of between about 10 nm to 50 nm (col. 3, line 6-11) (claims 4, 10, 13 and 16). Lin teaches that a second relaxed SiGe forms on the first silicon cap and forming a second tensile-strained silicon cap on the second relaxed SiGe layer (col. 3, lines 12-58) (claim 11). Lin teaches that the forming a second relaxed SiGe layer on the silicon substrate includes forming a relaxed SiGe layer to a thickness of between about 25 nm to 300nm (col.3, lines 12-47) (claim 12). Lin teaches that the forming a second tensile-strained silicon cap includes forming a second tensile-strained silicon cap having a thickness of between about 10 nm to 50 nm (col. 3, lines 48-58) (claim 13).

Lin lacks anticipation only in not explicitly teaching that: 1) a first relaxed SiGe layer is formed on the silicon substrate; and forming a first tensile-strained silicon cap on the first relaxed SiGe layer (claims 1 and 7); 2) the forming a first relaxed SiGe layer on the silicon substrate includes forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5 μm, and containing between about 10% and 100% Ge, and preferably between about 20% to 30% Ge (claims 3, 9 and 18); and 3) a first relaxed SiGe layer is formed on the silicon substrate, including forming a graded, relaxed SiGe layer to a thickness of between about 200 nm to 5μm, and containing between about 10% and 100% Ge, and preferably between about 20% to 30% Ge; and forming a first

tensile-strained silicon cap on the first relaxed SiGe layer having a thickness of between about 10 nm to 50 nm (claim 16).

Fitzgerald shows the formation of strained surface channel MOSFET devices with the use of a semiconductor heterostructure. In Fig. 2A we find a first relaxed SiGe layer (206) above a substrate (202) (col. 3, lines 44-54). Above the relaxed SiGe layer (206) we have a first strained silicon layer (208) (col. 3, lines 44-54). Additional relaxed SiGe layer (210) and strained silicon layer (212) are formed over the first the first heterostructure (col. 3, line 55-col. 4, line 6). Due to the lattice matching of the first SiGe layer and the second SiGe layer there is no limit to its thickness (col. 3, line 55-col. 4, line 6). The layers SiGe are formed with 10% to 100% of Ge and also forms the layer between the shorten range of 20% to 30% (col. 5, lines 36-43). This process is done to limit the decrease in carrier mobility and to positively affect device yield, reliability and performance (col. 2, lines 37-53).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Lin by forming a first relaxed SiGe layer and a first strained silicon cap, where the SiGe layer is formed with a Ge concentration of between 20% to 30%, as taught by Fitzgerald with the motivation that Fitzgerald teaches a process that limits the decrease in carrier mobility and to positively affect device yield, reliability and performance.

Lin as modified by Fitzgerald show the method substantially as claimed and as described in the preceding paragraph.

Lin as modified by Fitzgerald lacks anticipation only in not explicitly teaching that: 1) a silicon substrate is prepared, including doping a bulk silicon (100) substrate with ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates (claims 1, 7 and 16).

Chidambarrao shows a method for forming a strained silicon NMOS device with embedded source/drain regions. A CMOS device is formed here with a Si/SiGe structure on a silicon substrate that is prepared to form an NFET device (col. 3, line 14-24). This allows for both a small external resistance and a small channel resistance, creating a higher performance NFET (col. 1, line 59-col. 2, line 4).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Lin as modified by Fitzgerald by preparing a silicon substrate, including doping a bulk silicon (100) substrate with ions taken from the group of ions to form a doped substrate taken from the group of doped substrates consisting of n-type doped substrates and p-type doped substrates, as taught by Chidambarrao, with the motivation that Chidambarrao teaches that this allows for both a small external resistance and a small channel resistance, creating a higher performance NFET.

Note Welser* can also be use as it teaches the formation of a heterostructure device formed over a doped substrate.

Allowable Subject Matter

6. Claims 2, 14 15, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...selectively laterally etching of any SiGe layer at the source and drain region and selectively laterally etching of any SiGe layer located beneath the gate and nitride spacers, forming a resulting tunnel, which is left empty or filled with a dielectric, as required by claims 2, 14 15, 20 and 21, respectively as they depend from claims 1, 11 16 and 17 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
June 2, 2005